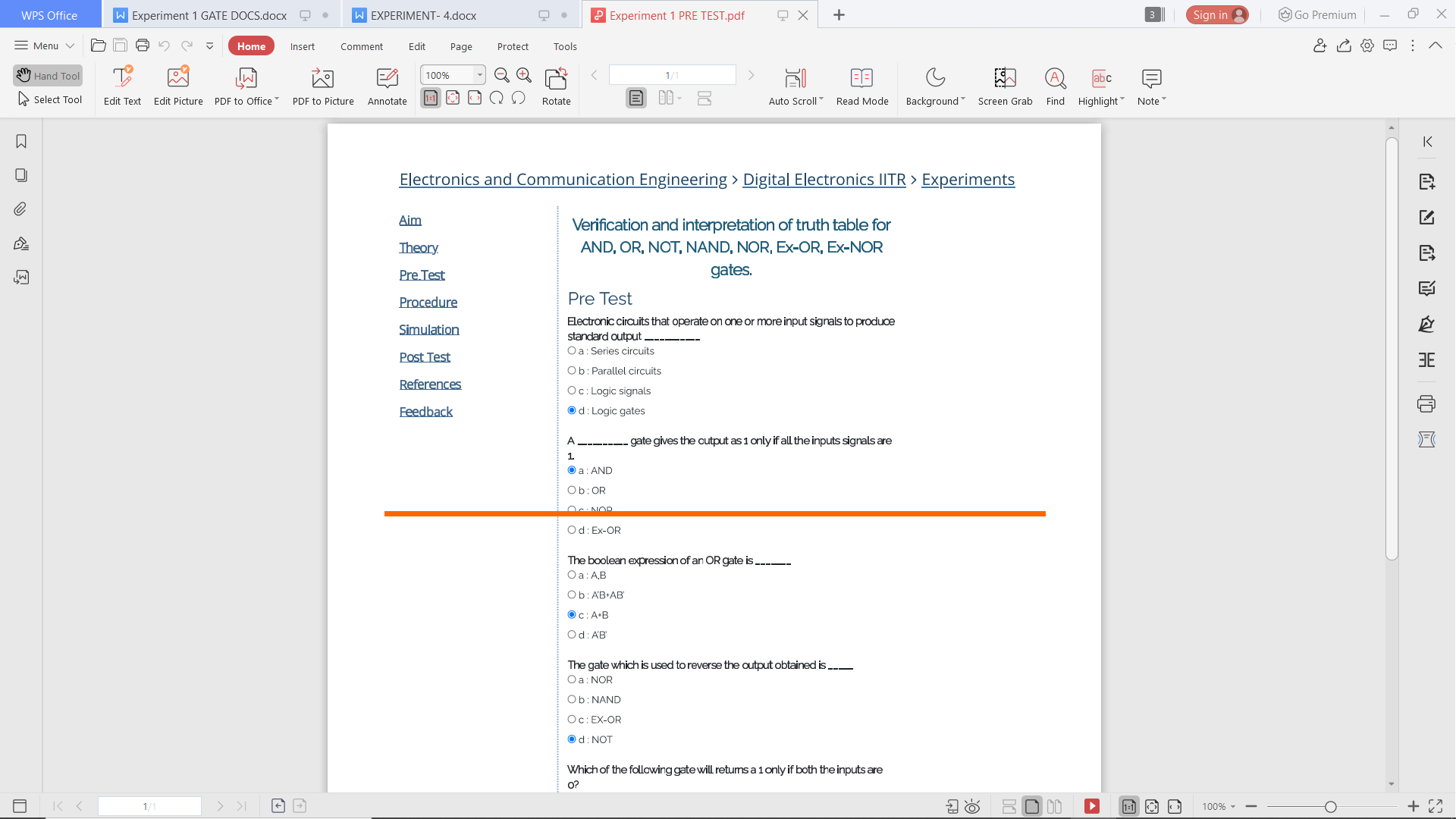
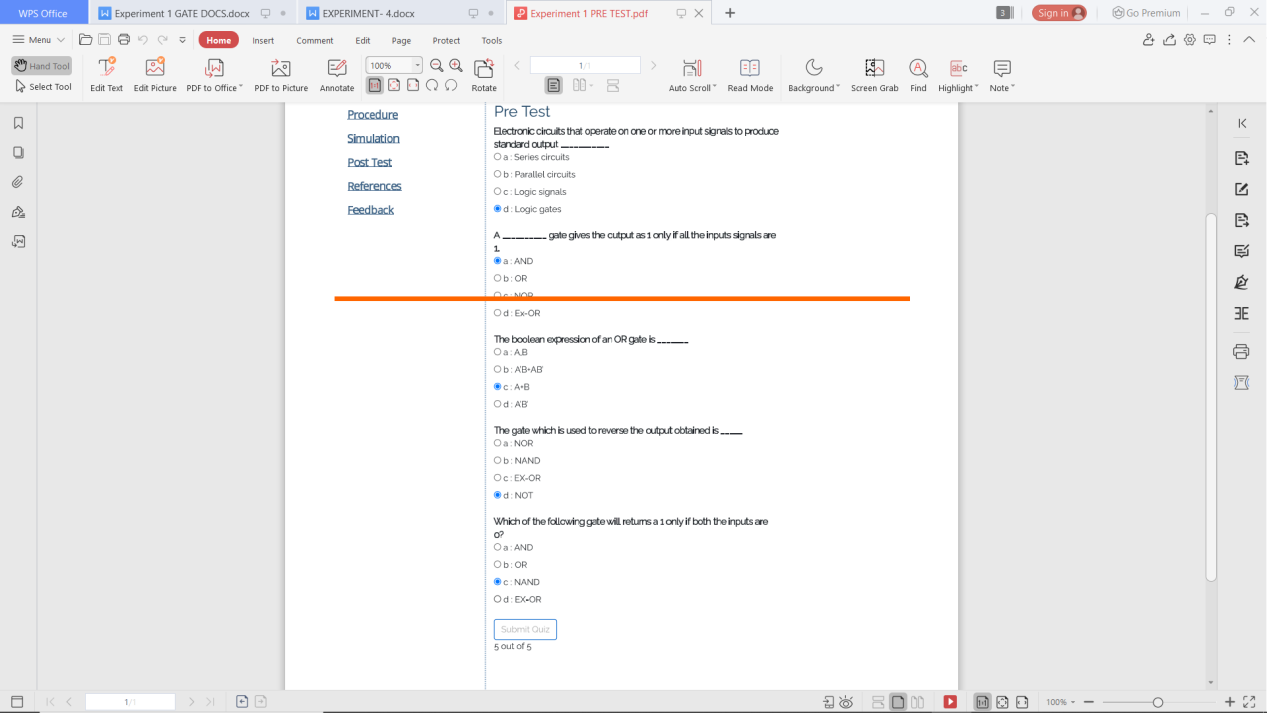
**EXPERIMENT- 1**

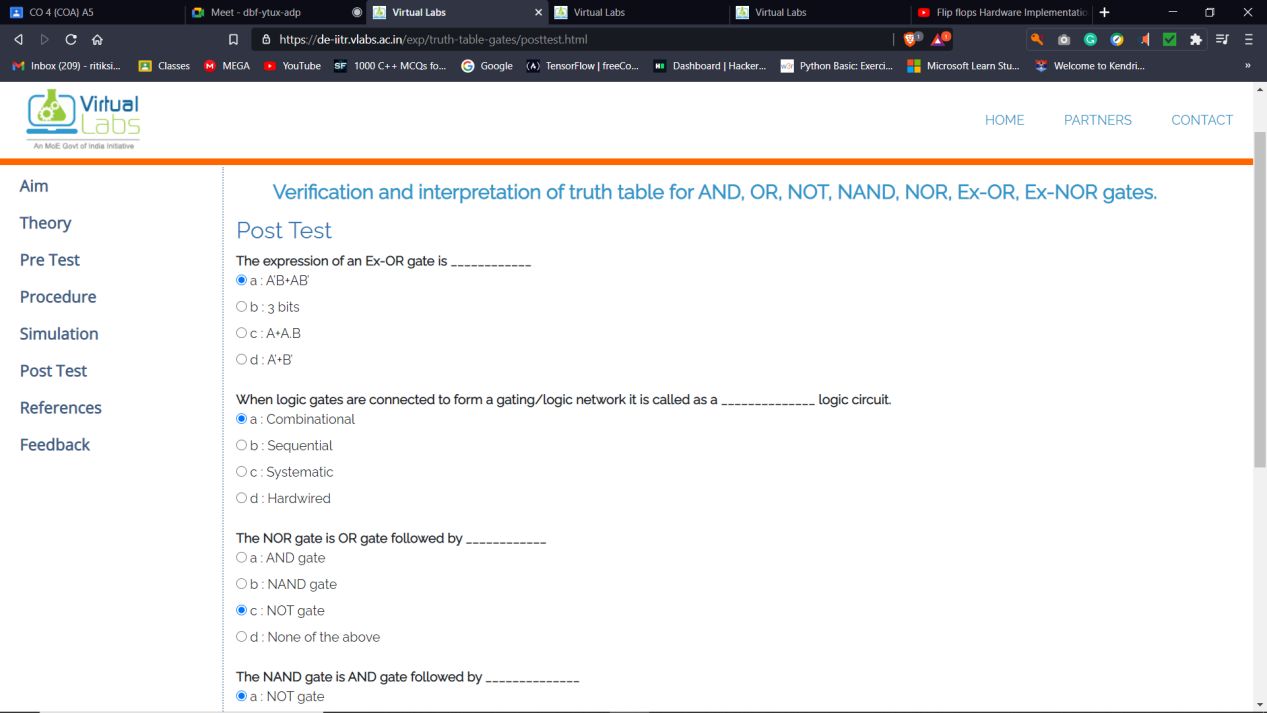
## Aim: Verification and interpretation of truth table for AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates.

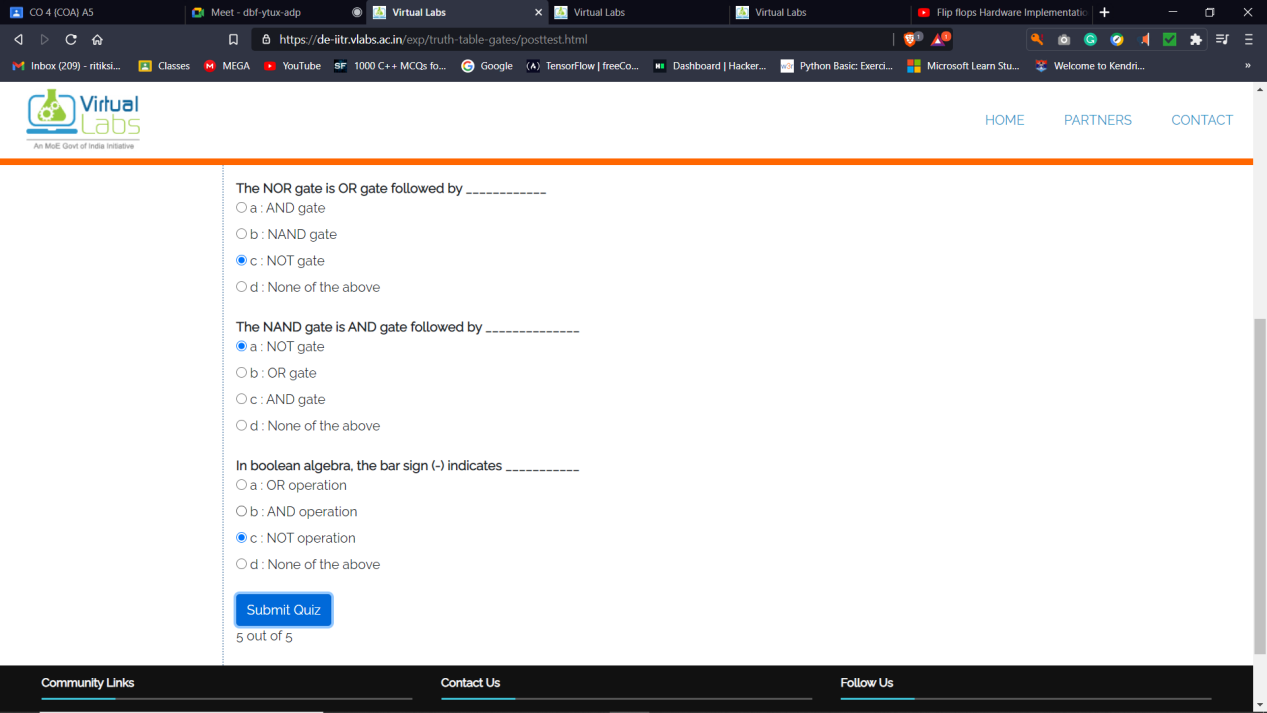
* **PRE TEST**

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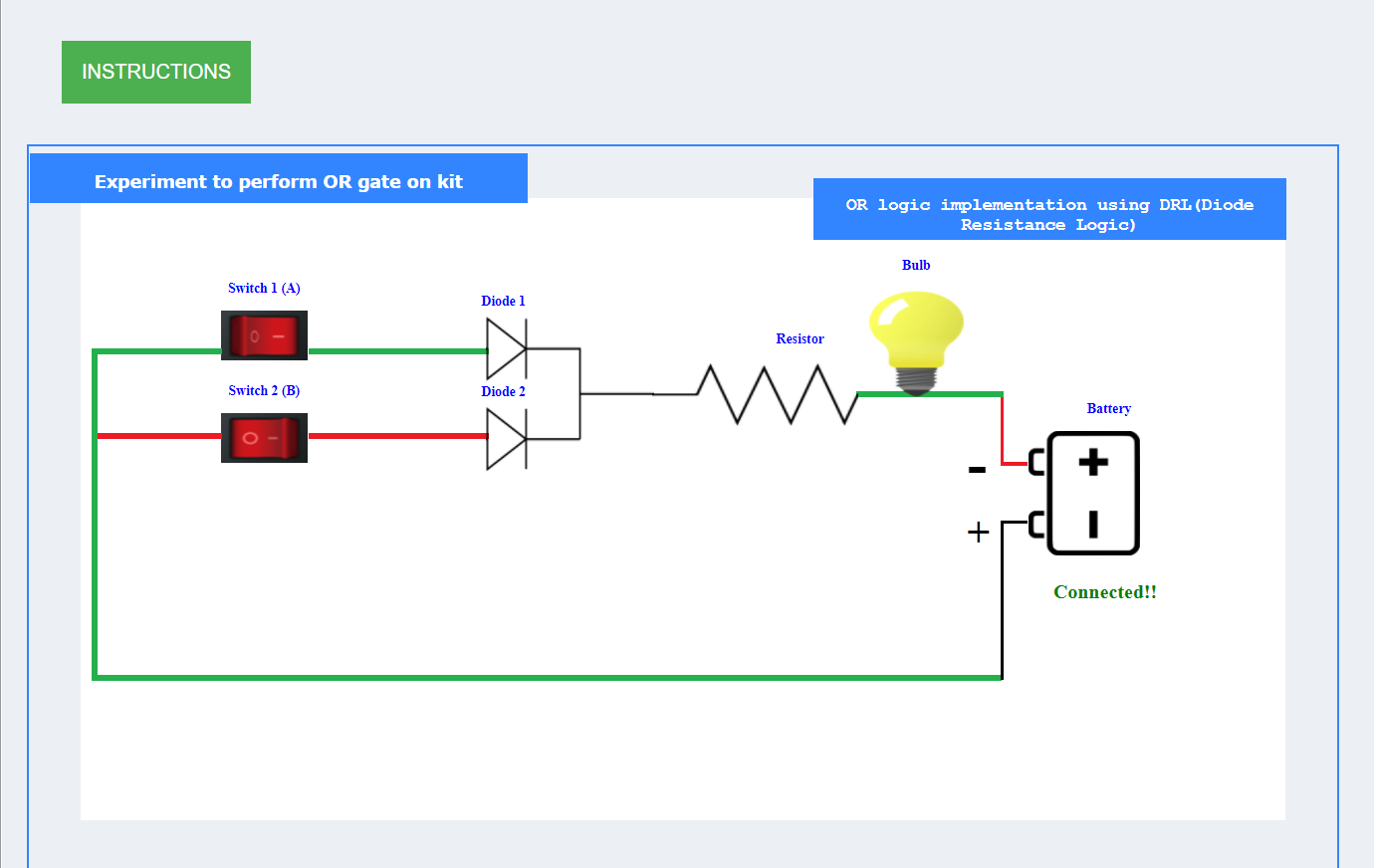
* **POST TEST**

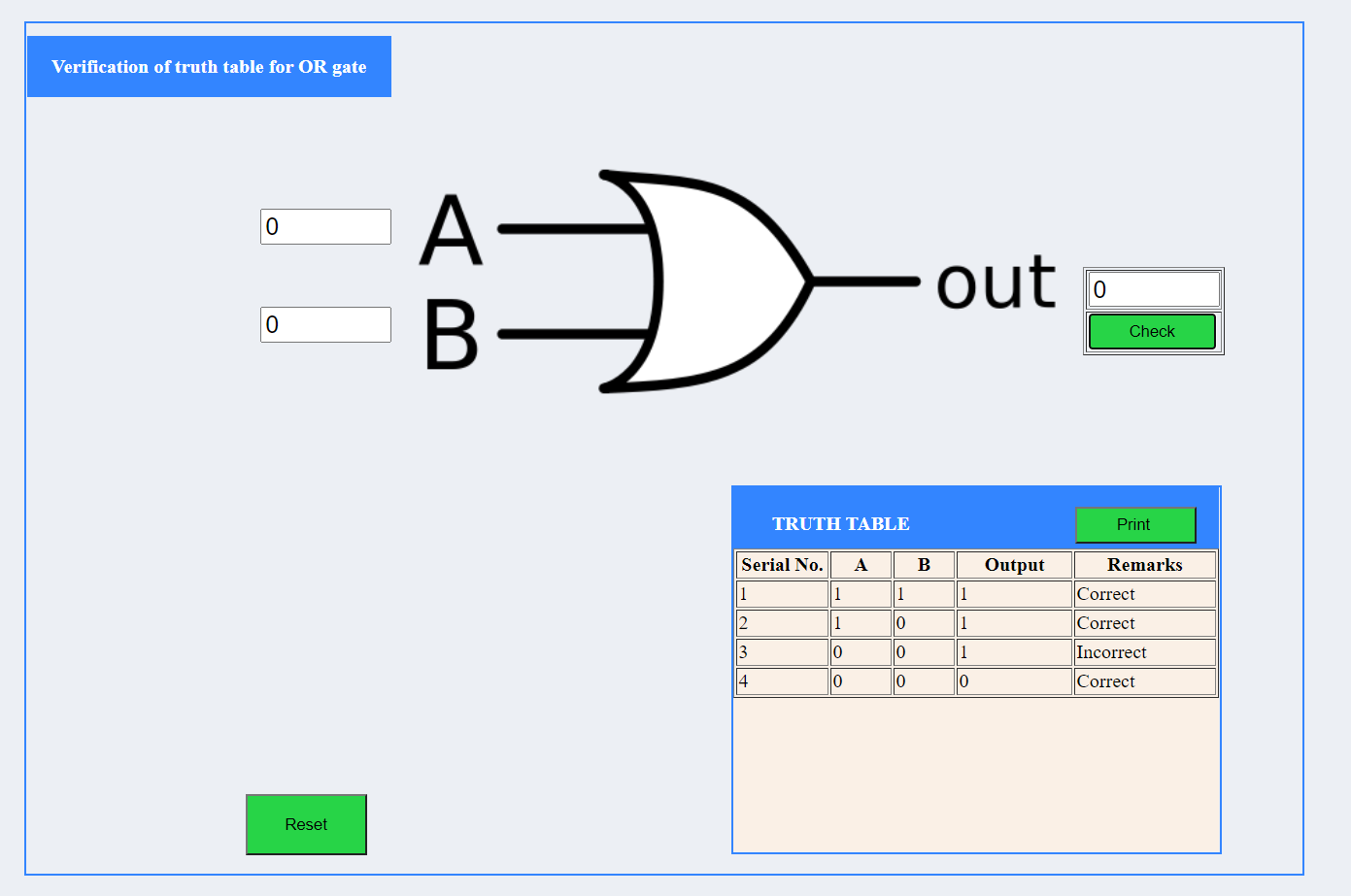
****

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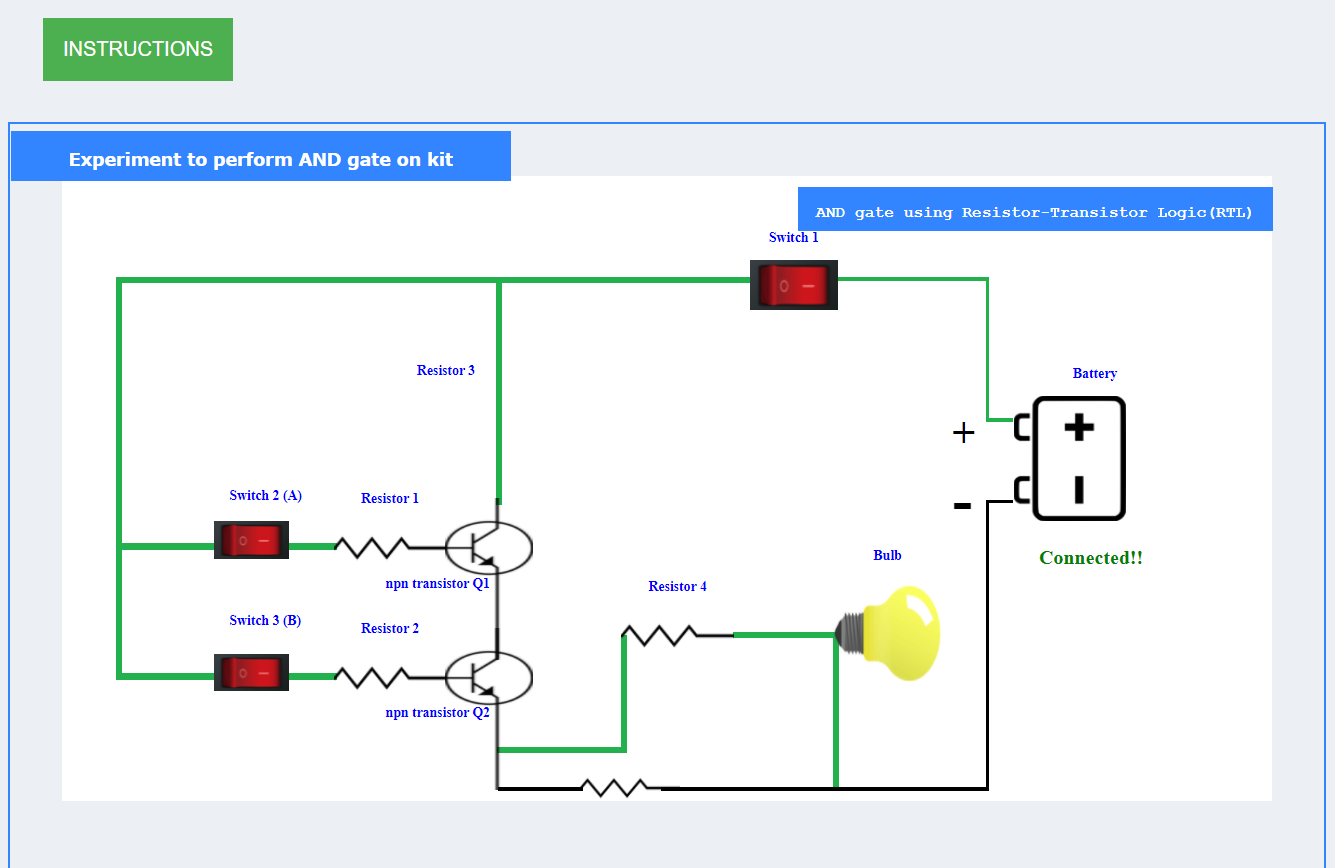
* **SIMULATION**

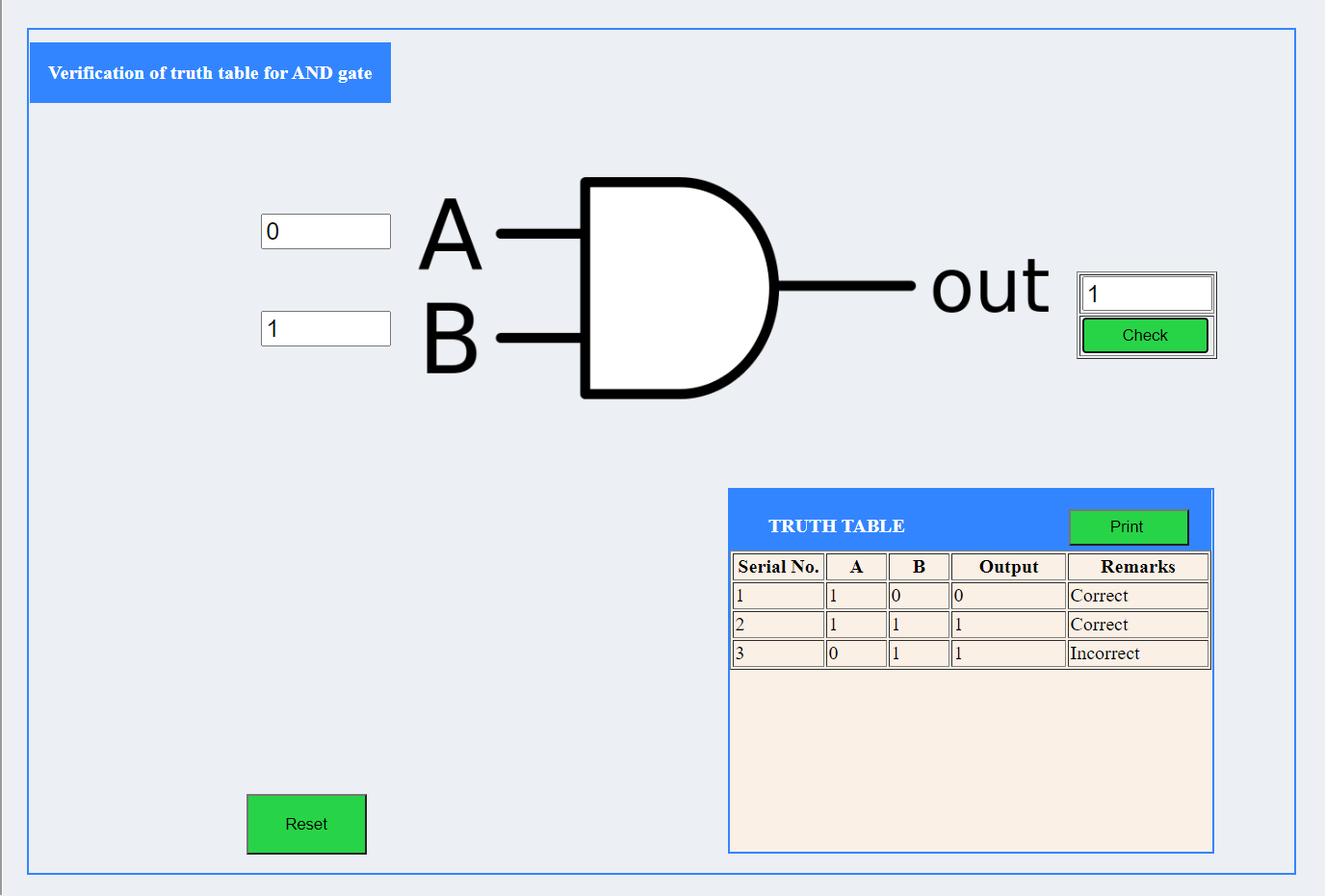
**OR GATE**



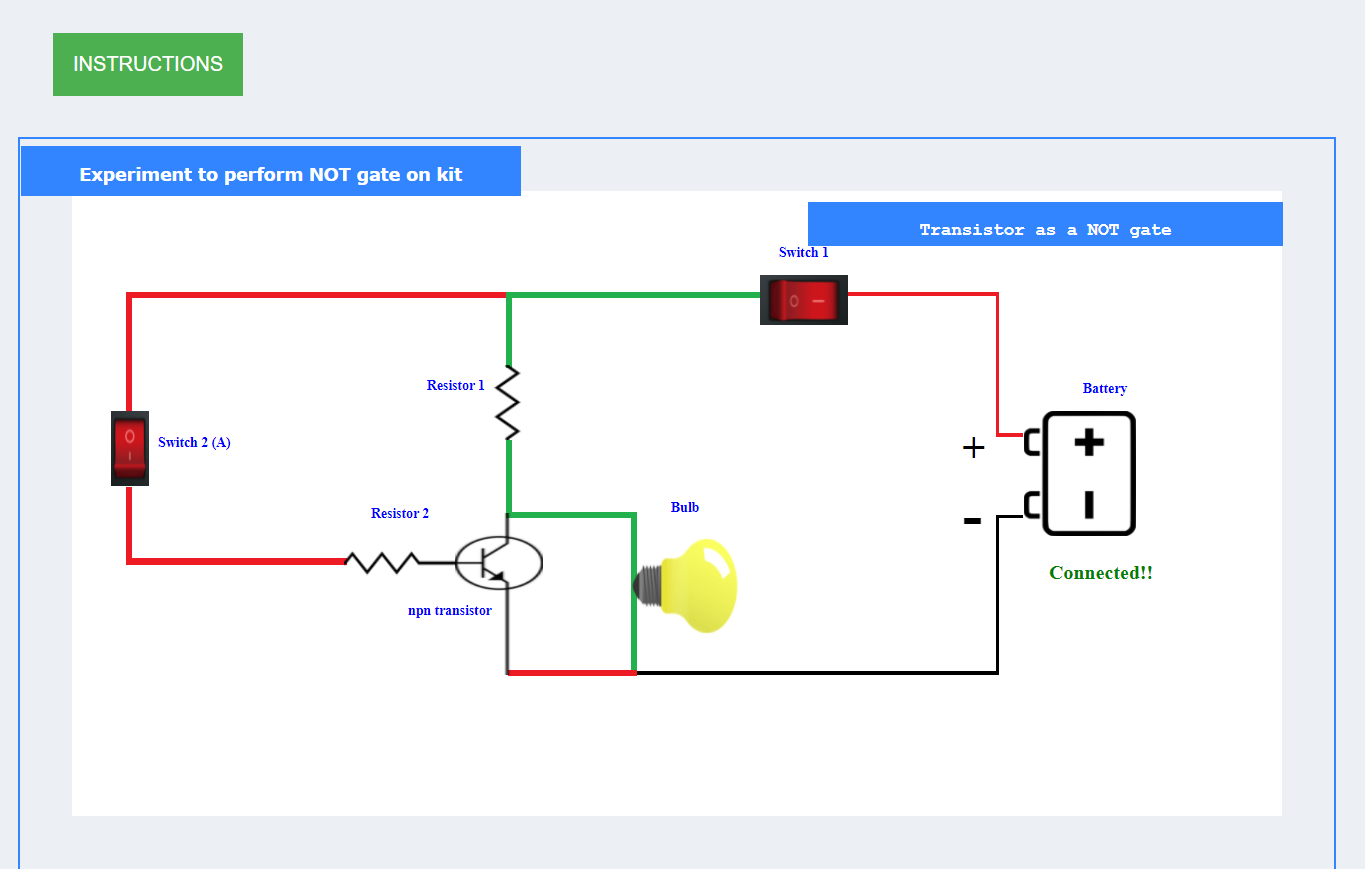


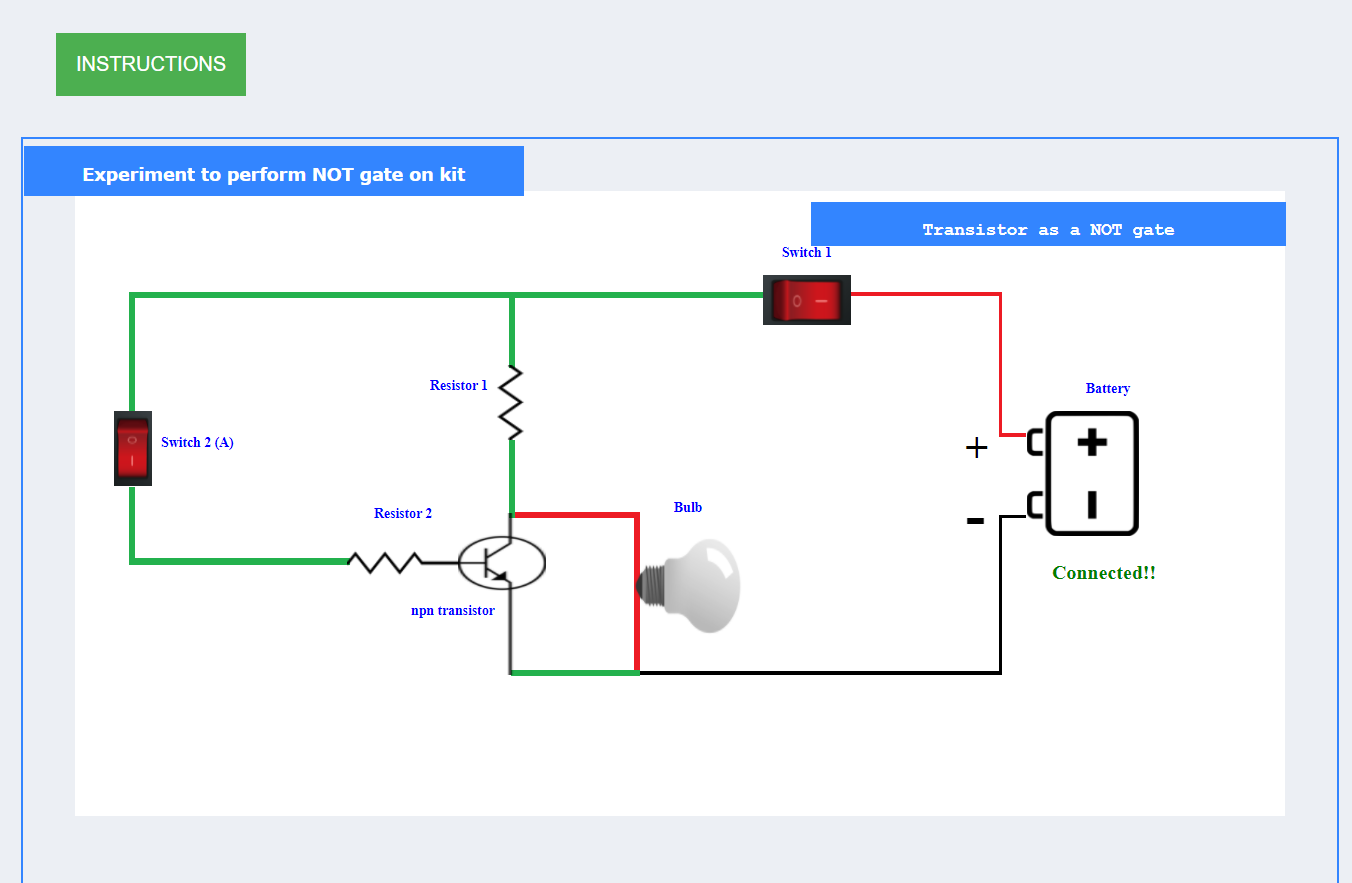
**AND GATE**

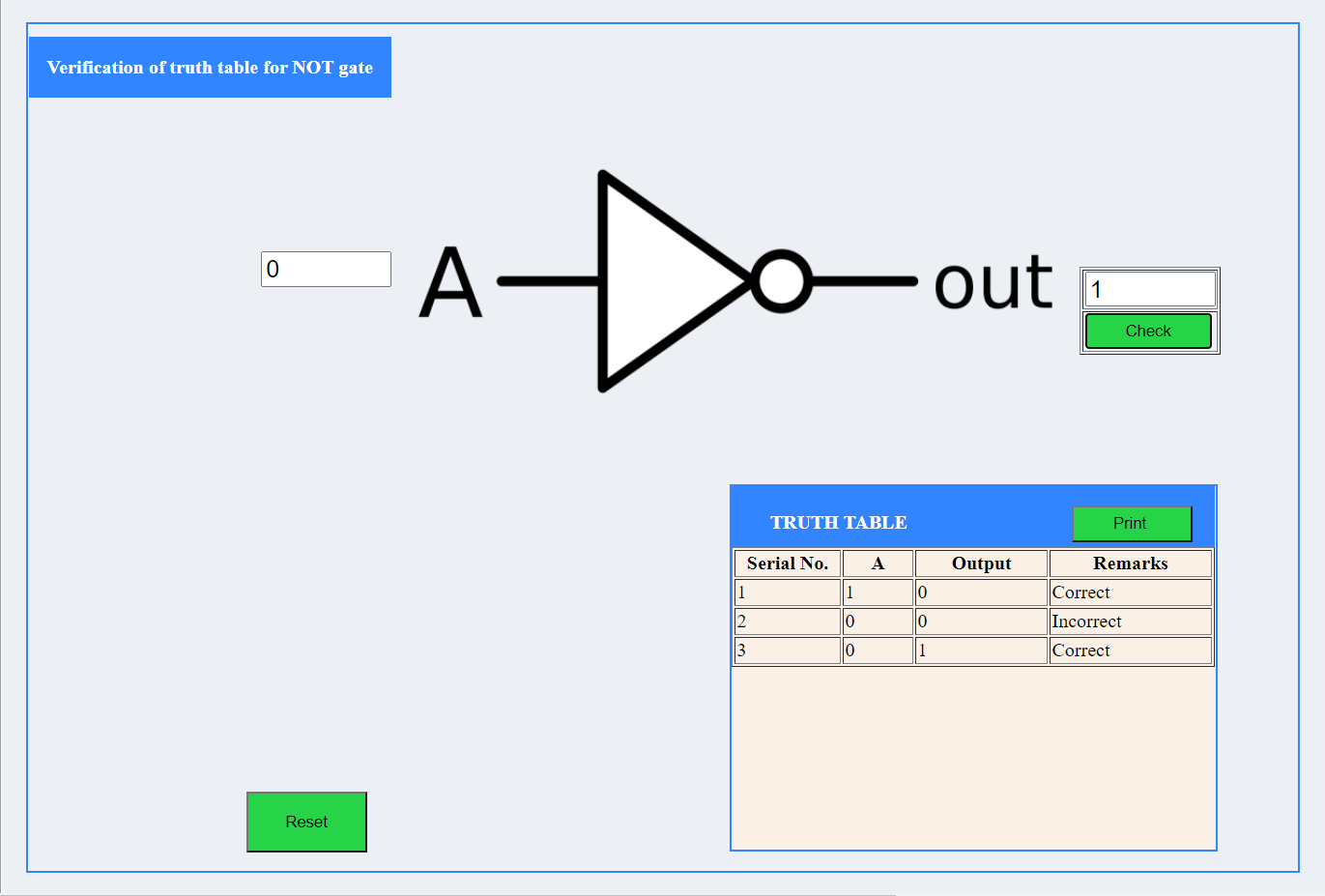




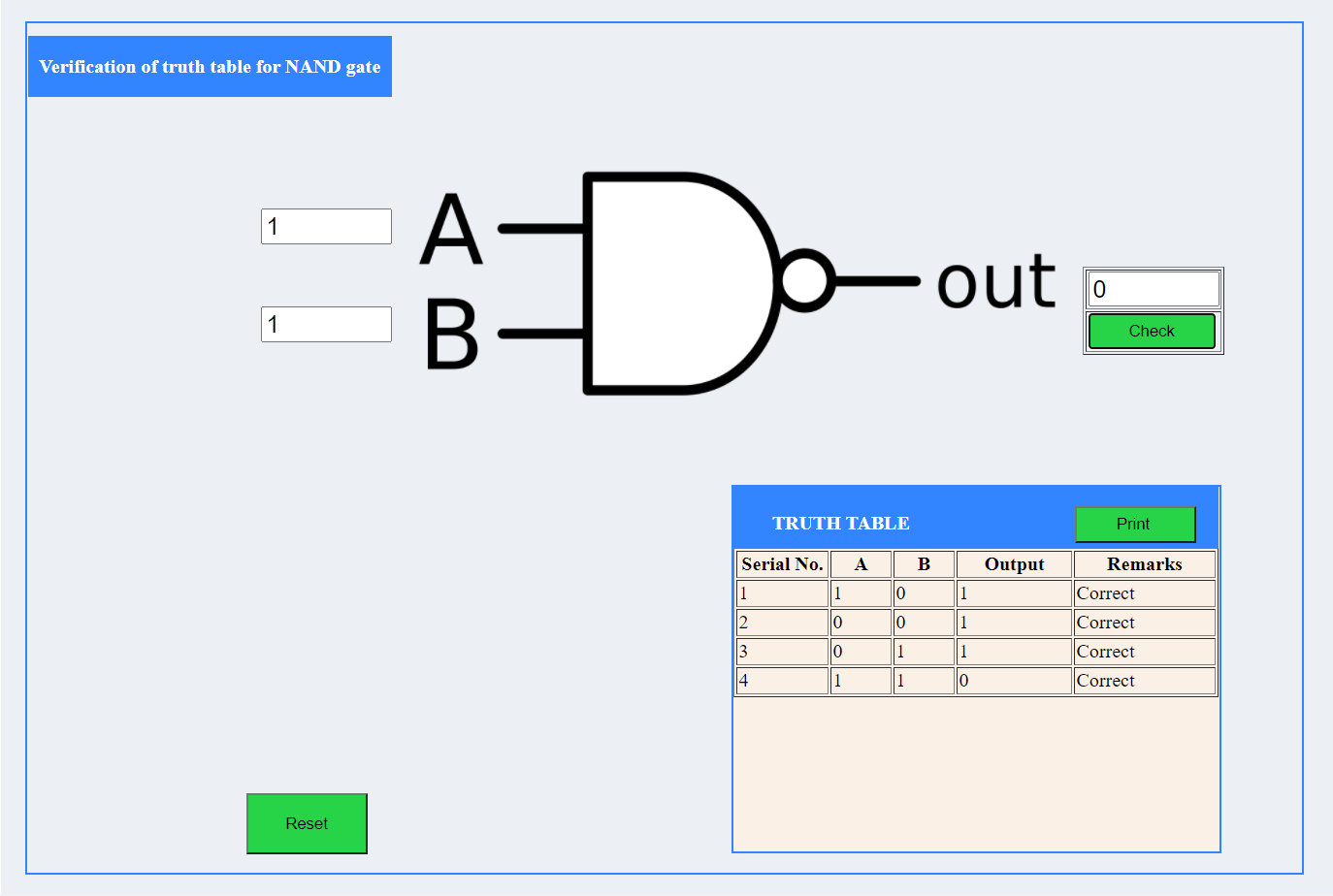
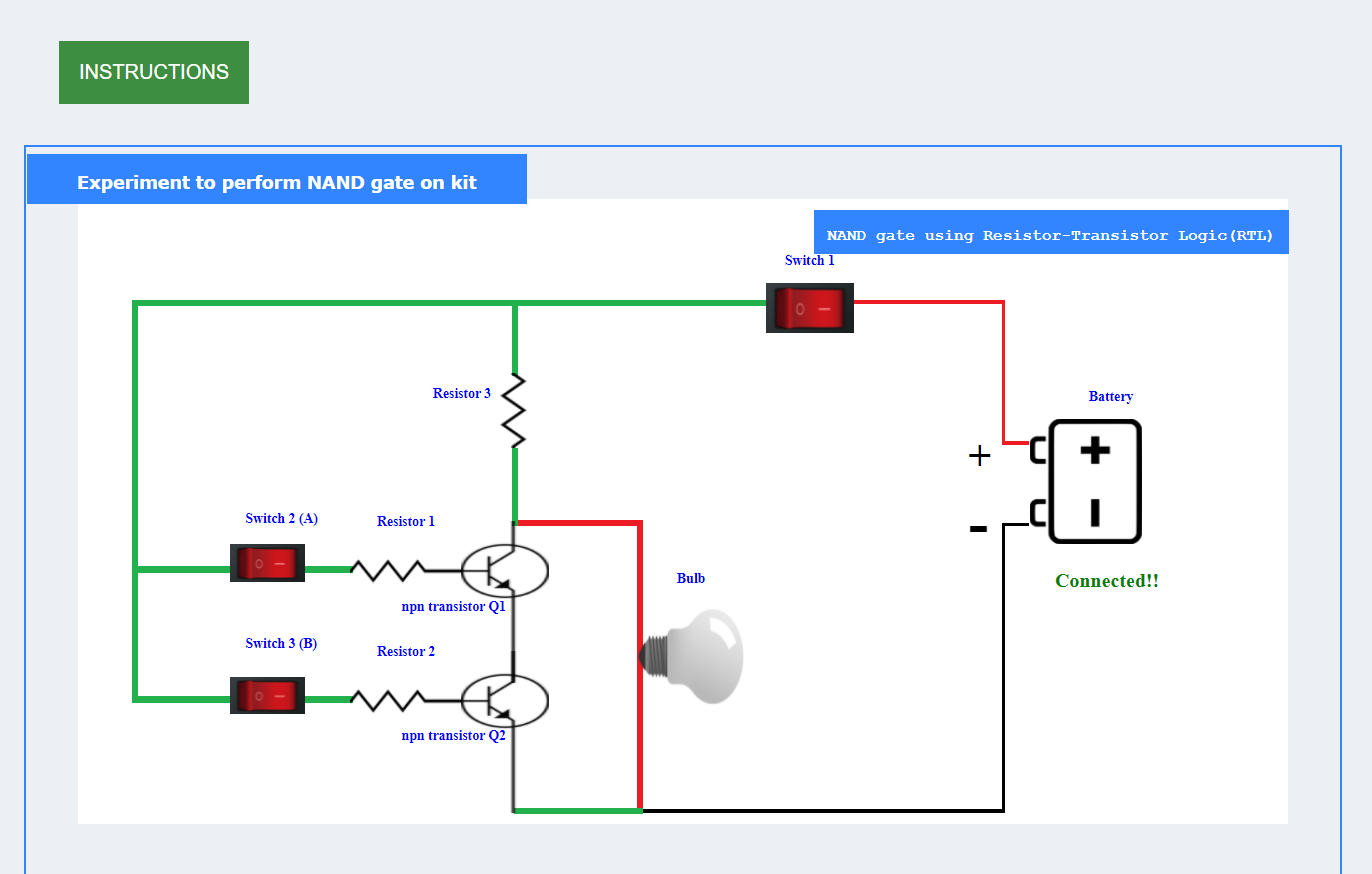
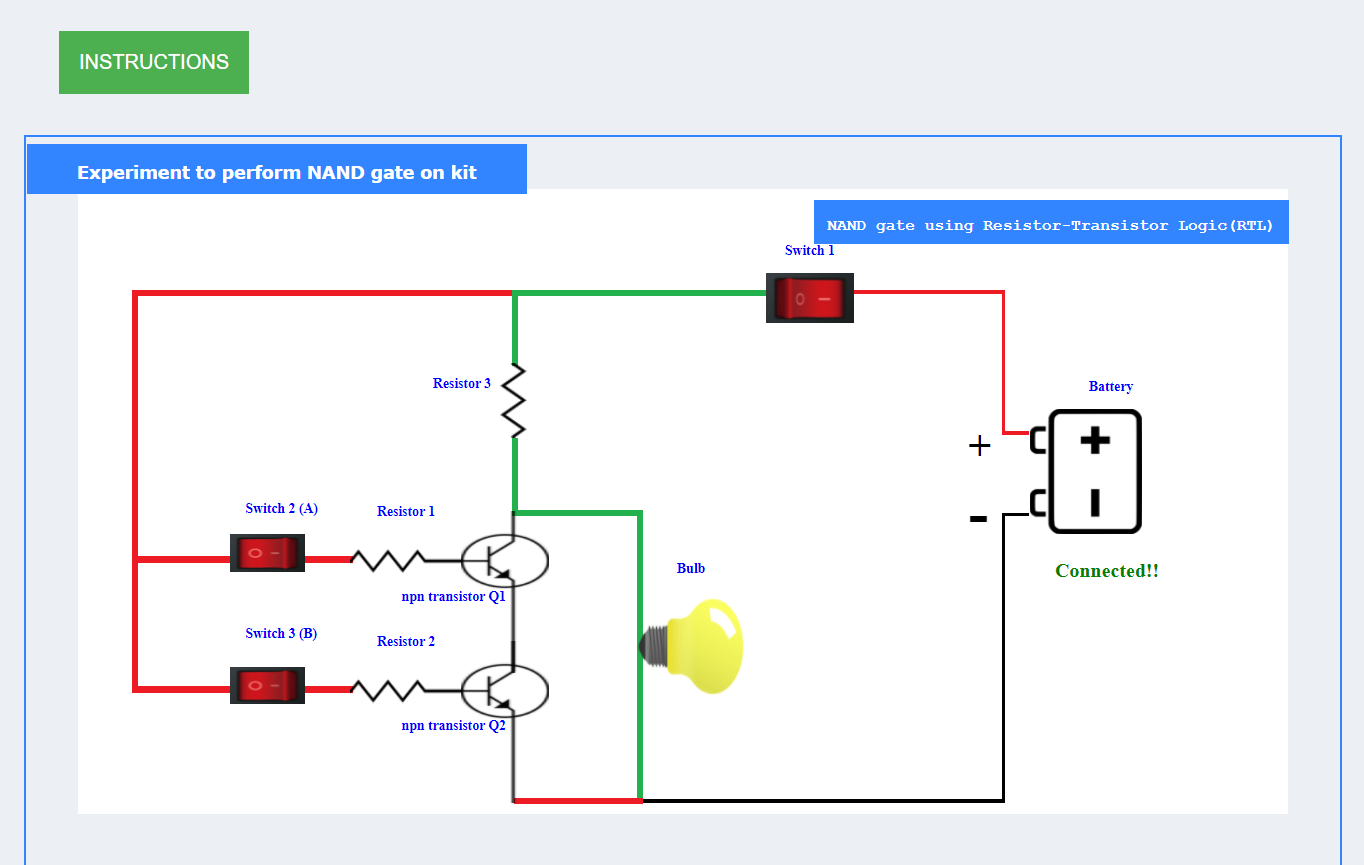
**NOT GATE**



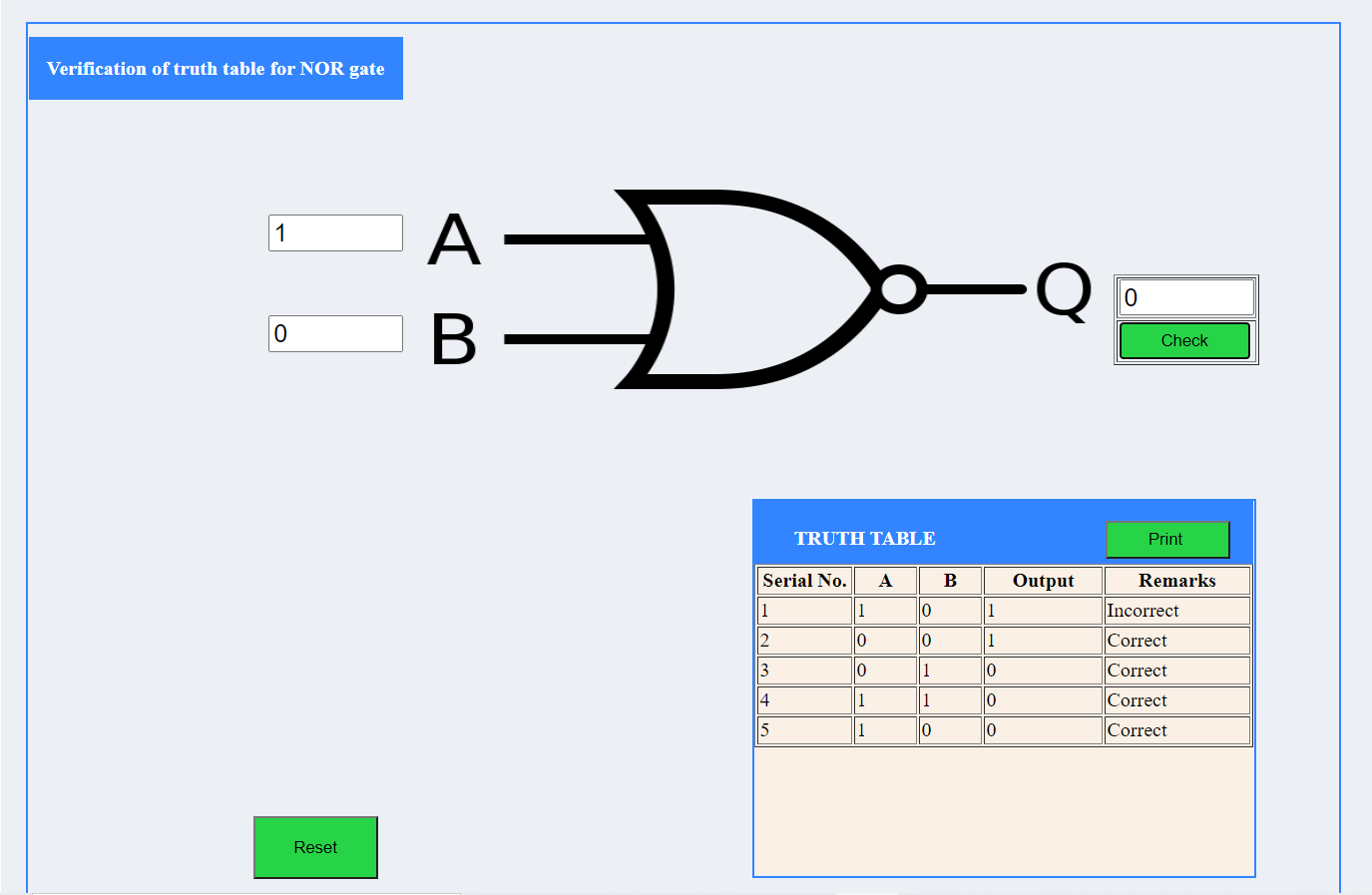
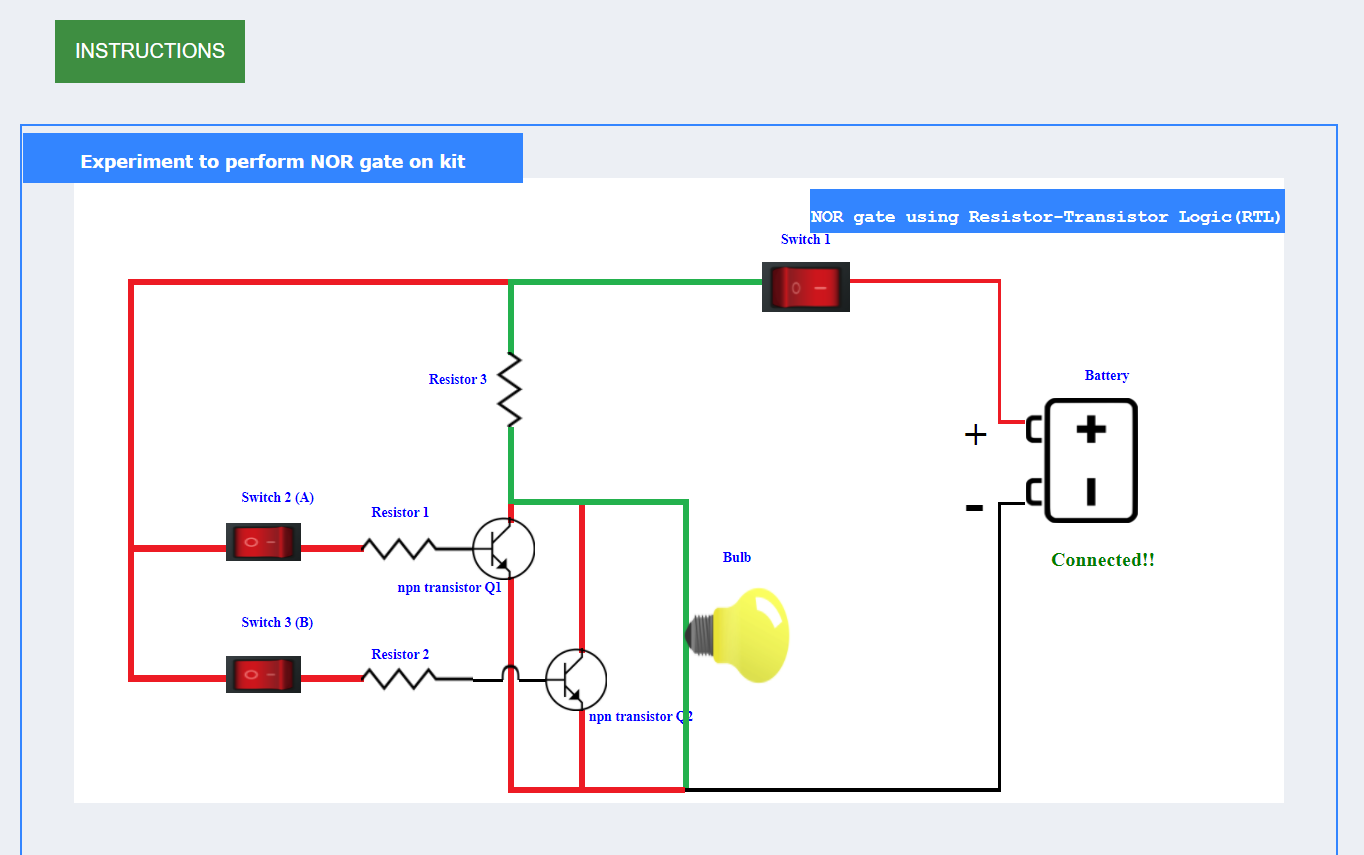
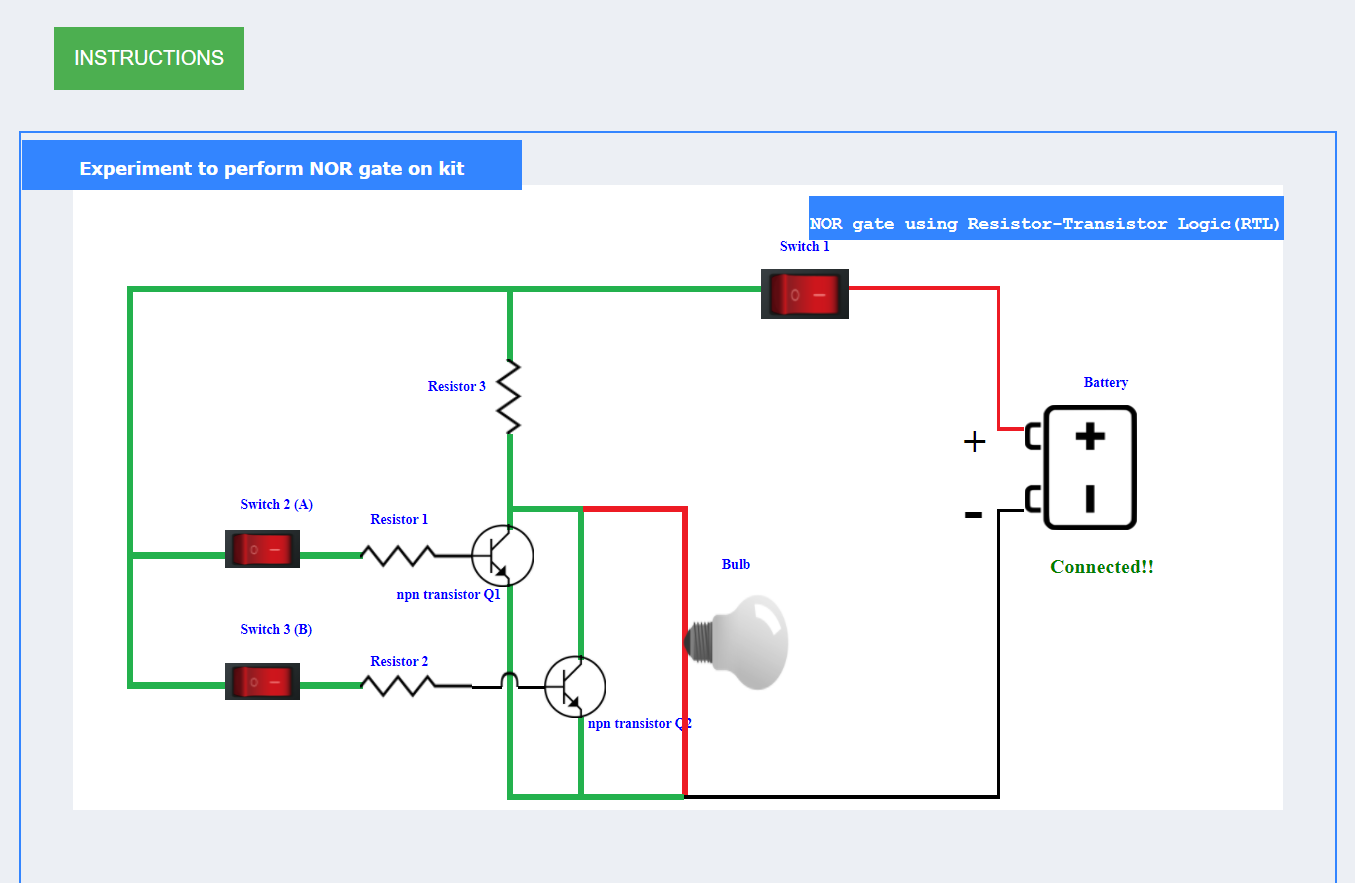


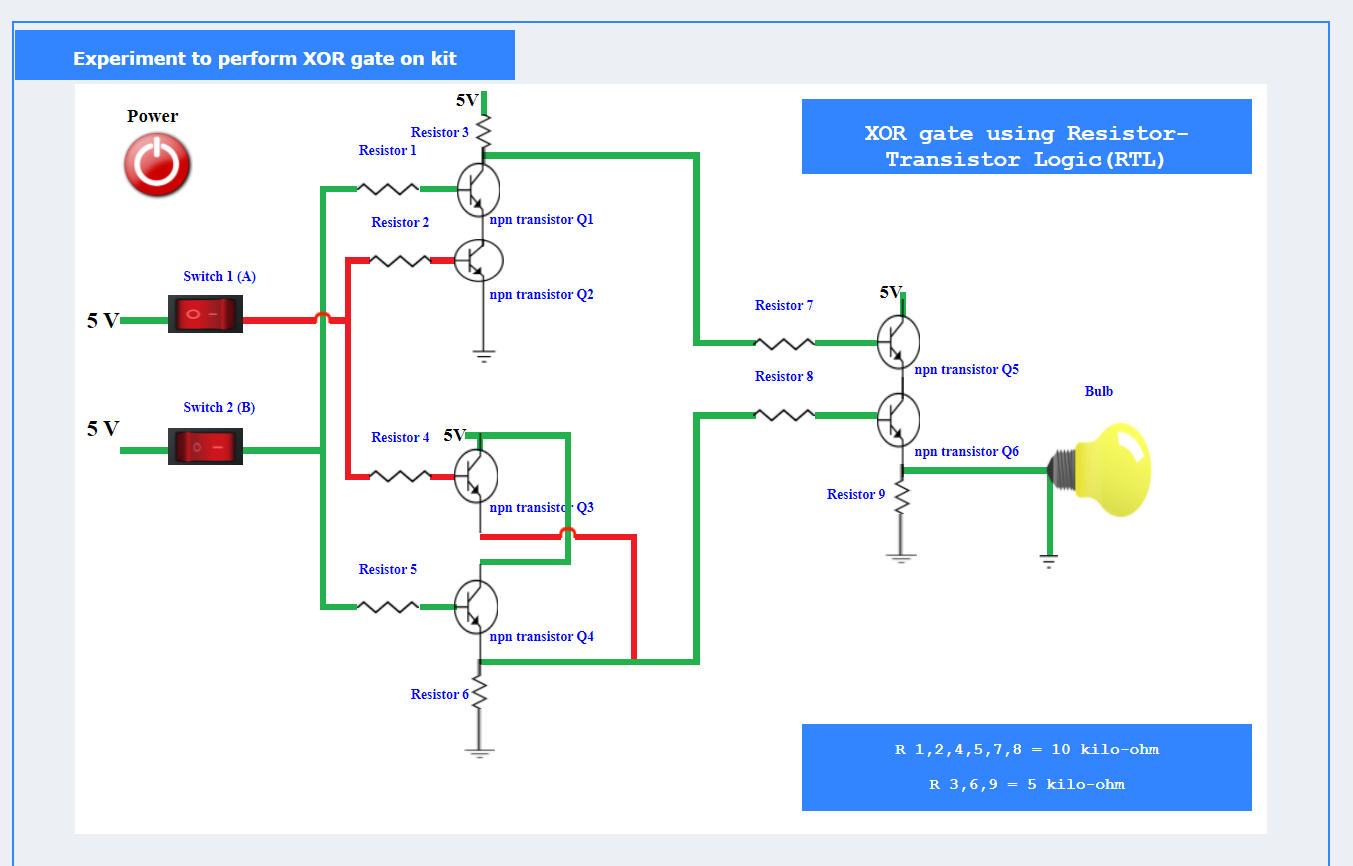
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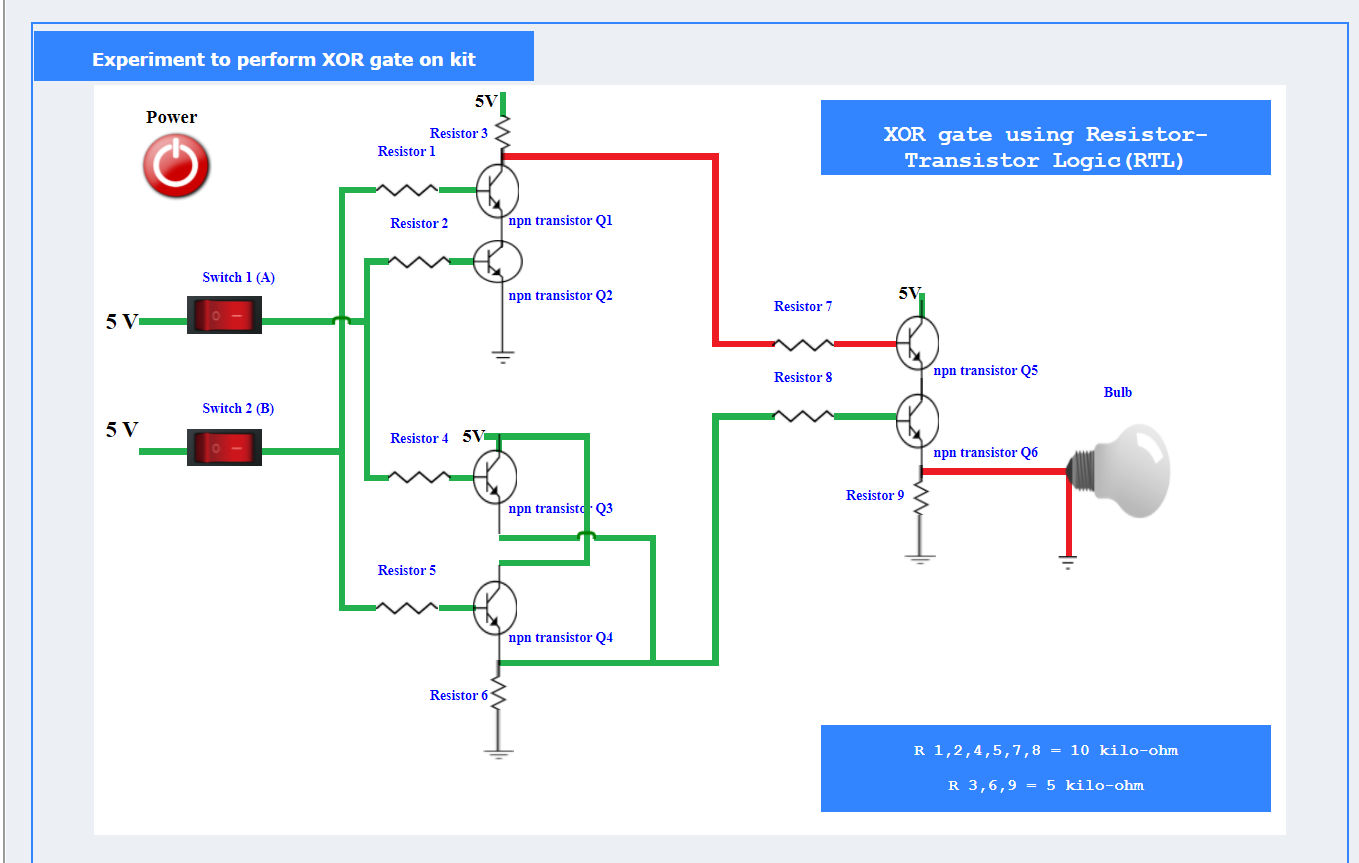
**NAND GATE**

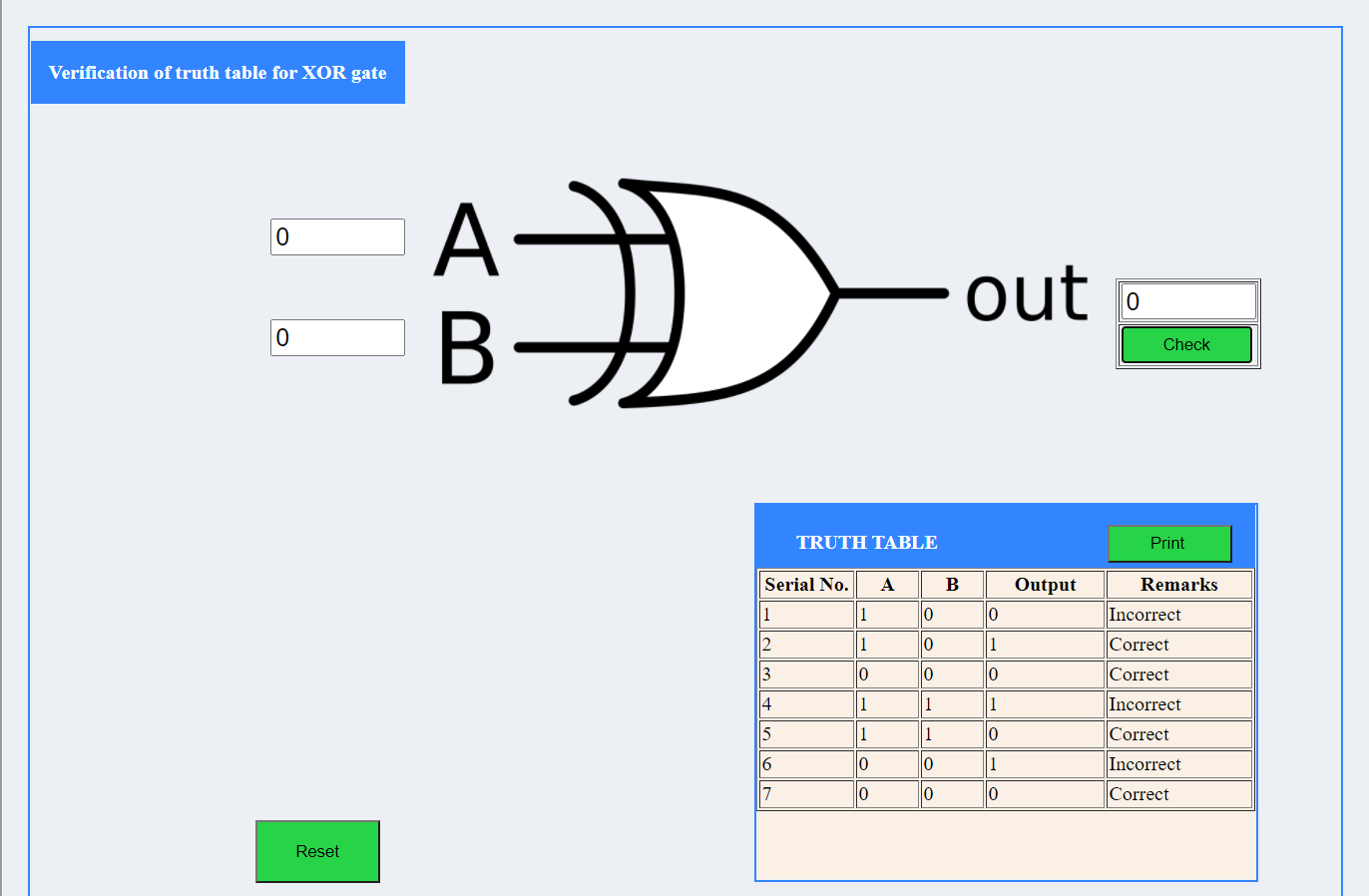


**NOR GATE**



**XOR GATE** 





**XNOR GATE** 